FICER Technology Co., Ltd.
明虹科技股份有限公司

2F, No.138, Daye Rd., Beitou Dist.,
Taipei City 11268, Taiwan
www.Ficer.com

SKU: 02W0K04

100G QSFP28 ZR4 Dual-Rate Transceiver
Hot Pluggable, Duplex LC, LAN-WDM EML, SMF 80KM, DDM

Part Number: FQ28-K7-L13-80DR

Overview

FQ28-K7-L13-80DR is a 4-Channel LWDM 1300nm QSFP28 transceiver for 100GbE and OTU4 applications especially in Telecom, Datacom, Data Center & Storage networks. The transmitter converts 4-Channel 25/28G electrical input data to four LWDM optical signals and multiplex that into one 103/112G signal. The receiver de-multiplex the 103/112G signal reversely and converts that to 4-Channel 25/28G electrical output data. The techniques bring a compact transceiver module for an aggregate bandwidth of 103/112Gbps up to SMF 80km optical links.

Applications

- 100GBASE-ZR4 Ethernet
- OTN OTU4 @112.1G
- Data Centers Switch Interconnect
- Server and Storage Area Network Interconnect

Features

- Compatible with IEEE802.3ba 100GBASE-ER4
- Compatible with ITU G.959.1 OTU4 4L1-9D1F
- Compliant with SFF-8665 QSFP28 MSA
- Compliant with IEEE 802.3bm CAUI-4 Interface
- 4CH LWDM MUX / DEMUX design
- Data Rate up to 27.9525Gbps per Lane
- Built in quad Tx CDR and Rx CDR
- Hot Pluggable QSFP28 footprint
- O-Band LWDM EML transmitter
- SOA + PIN receiver
- Duplex LC connector
- 2-wire interface for management and diagnostic monitor compliant with SFF-8636
- Single 3.3V power supply
- Link distance 80km over SM fiber with FEC
- Link distance 60km over SM fiber without FEC
- Maximum Power consumption 6.5W
- RoHS compliant

TEL+886-2-2898-3830 FAX+886-2-2898-3840 Sales@Ficer.com

Laser Safety

- This is a Class 1 Laser Product complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.
- Caution: Use of control or adjustments or performance of procedure other than those specified herein may result in hazardous radiation exposure.

Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Storage Temperature	T_{ST}	-40	+85	°C
Storage Relative Humidity	RH	0	85	%
Supply Voltage	V_{CC3}	-0.5	+3.6	V

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Unit
Case Operating Temperature	T_{OP}	0	-	+70	°C
Supply Voltage	V_{CC}	+3.13	+3.3	+3.47	V
Data Rate, per Lane	DR		25.78125	27.9525	Gb/s
Data Rate Accuracy (100GBASE-ZR4)	ΔDR	-100		+100	ppm
Data Rate Accuracy (OTU4 4L1-9D1F)	ΔDR	-20		+20	ppm
Bit Error Rate	BER			$5x10^{-5}$	
Supply Current	I_{CC}			1900	mA
Power Consumption	P			6.5	W
Transceiver Power-on Initialization Time				2000	ms
Control Input Voltage High	V_{IH}	2.0		Vcc	V
Control Input Voltage Low	V_{IL}	GND		0.8	V
Control Output Voltage High	V_{OH}	2.0		Vcc	V
Control Output Voltage Low	V_{OL}	GND		0.8	V

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Transmitter Electro-optical Characteristics

V_{CC} = 3.13V to 3.47V, T_{OP} = 0 °C to 70 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
100GBASE-ZR4						
Operating Data Rate, per Lane	DR		25.78125		Gb/s	
Total Average Launch Power	TP_{AVG}			+12.5	dBm	
Average Launch Power, per Lane	P_{AVG}	+2		+6.5	dBm	
Optical Modulation Amplitude (OMA), per Lane	P_{OMA}	+3		+6.5	dBm	1
Difference in Launch Power between any two Lanes (OMA)	$P_{TX-DIFF}$			3.6	dB	
Transmitter Dispersion Penalty, per Lane	TDP			3	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), per Lane	OMA-TDP	1.3			dB	1
ITU G.959.1 OTU4 4L1-9D1F						
Operating Data Rate, per Lane	DR		27.9525		Gb/s	
Total Average Launch Power	TP_{AVG}			+12.5	dBm	
Average Launch Power, per Lane	P_{AVG}	+3.8		+6.5	dBm	
100GBASE-ZR4 & ITU G.959.1 OTU4 4L1-9D1F						
Optical Wavelength, each Lane	λ_{L0}	1294.53	1295.56	1296.59	nm	
	λ_{L1}	1299.02	1300.05	1301.09	nm	
	λ_{L2}	1303.54	1304.58	1305.63	nm	
	λ_{L3}	1308.09	1309.14	1310.19	nm	
Spectral Width (-20dB)	$\Delta\lambda$			1	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Optical Extinction Ratio	ER	7			dB	
Optical Eye Mask { X1, X2, X3, Y1, Y2, Y3 }		{ 0.25, 0.4, 0.45, 0.25, 0.28, 0.4 }				2
Average Launch Power OFF, per Lane	P_{OFF}			-30	dBm	
Relative Intensity Noise (OMA)	RIN			-130	dB/Hz	
Optical Return Loss Tolerance	ORLT			20	dB	
Transmitter Reflectance	R_{TX}			-12	dB	
Input Differential Impedance	Z_{IN}	90	100	110	Ω	
Differential Data Input Voltage	V_{IN-PP}	180		1000	mVpp	

Note1: Transmitter wavelength and launch power need to meet the OMA minus TDP specs to guarantee link performance.

Note2: Hit ratio $5x10^{-5}$ hits per sample.

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Receiver Electro-optical Characteristics

V_{CC} = 3.13V to 3.47V, T_{OP} = 0 °C to 70 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
100GBASE-ZR4						
Operating Data Rate, per Lane	DR		25.78125		Gb/s	
Average Receive Power, per Lane	P_{RX-AVG}	-28		-7	dBm	
Receiver Power (OMA), per Lane	P_{RX-OMA}			-7	dBm	
Receiver Sensitivity (OMA), per Lane	SEN_{OMA}			-27.5	dBm	1
Stressed Receiver Sensitivity (OMA), per Lane	SRS_{OMA}			-25.5	dBm	1
ITU G.959.1 OTU4 4L1-9D1F						
Operating Data Rate, per Lane	DR		27.9525		Gb/s	
Average Receive Power, per Lane	P_{RX-AVG}	-26.4		-7	dBm	2
Equivalent Sensitivity, per Lane	SEN_{EQV}			-28	dBm	2
Optical Path Penalty				3	dB	
100GBASE-ZR4 & ITU G.959.1 OTU4 4L1-9D1F						
Damage Threshold, per Lane	D_{TH}	+6.5			dBm	3
Receiver Reflectance	R_{RX}			-26	dB	
LOS De-Assert	LOS_D			-29	dBm	
LOS Assert	LOS_A	-40			dBm	
LOS Hysteresis	LOS_{HY}	0.5			dB	
Receiver Electrical 3dB upper Cutoff Frequency, each Lane	F_{CUT}			31	GHz	
Output Differential Impedance	Z_{OUT}	90	100	110	Ω	
Differential Data Output Voltage	V_{OUT-PP}			900	mVpp	
Conditions of Stress Receiver Sensitivity Test (Note.4)						
Vertical Eye Closure Penalty, per Lane	VECP		1.5		dB	
Stressed Eye J2 Jitter, per Lane	J2		0.3		UI	
Stressed Eye J9 Jitter, per Lane	J9		0.47		UI	

Note1: Measured with conformance test signal at receiver input for BER= $5x10^{-5}$.

Note2: Measured with conformance test signal at receiver input for BER = $1x10^{-6}$ per ITU-OTU4 with Tx ER > 7dB

Note3: The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

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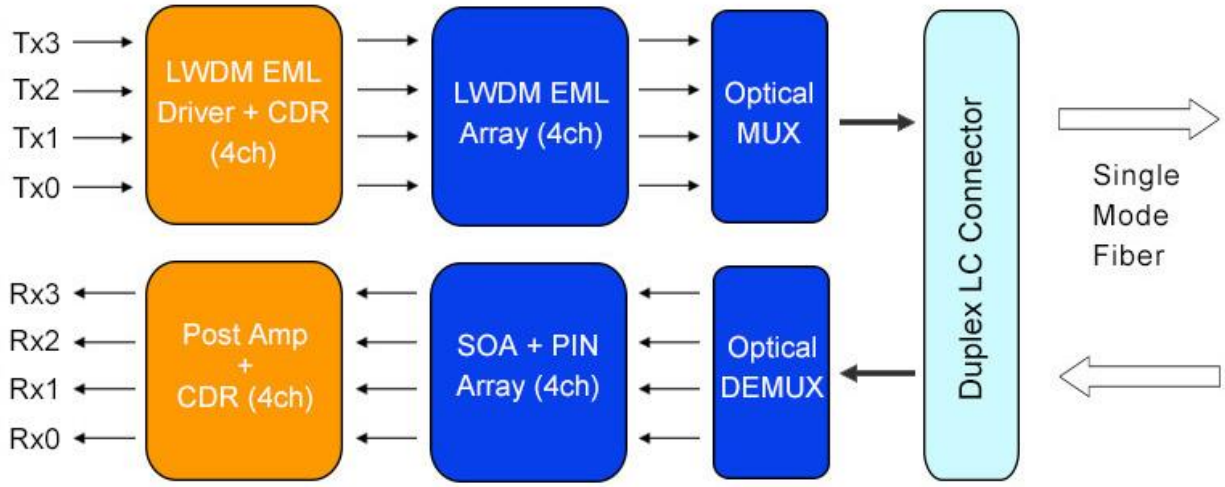
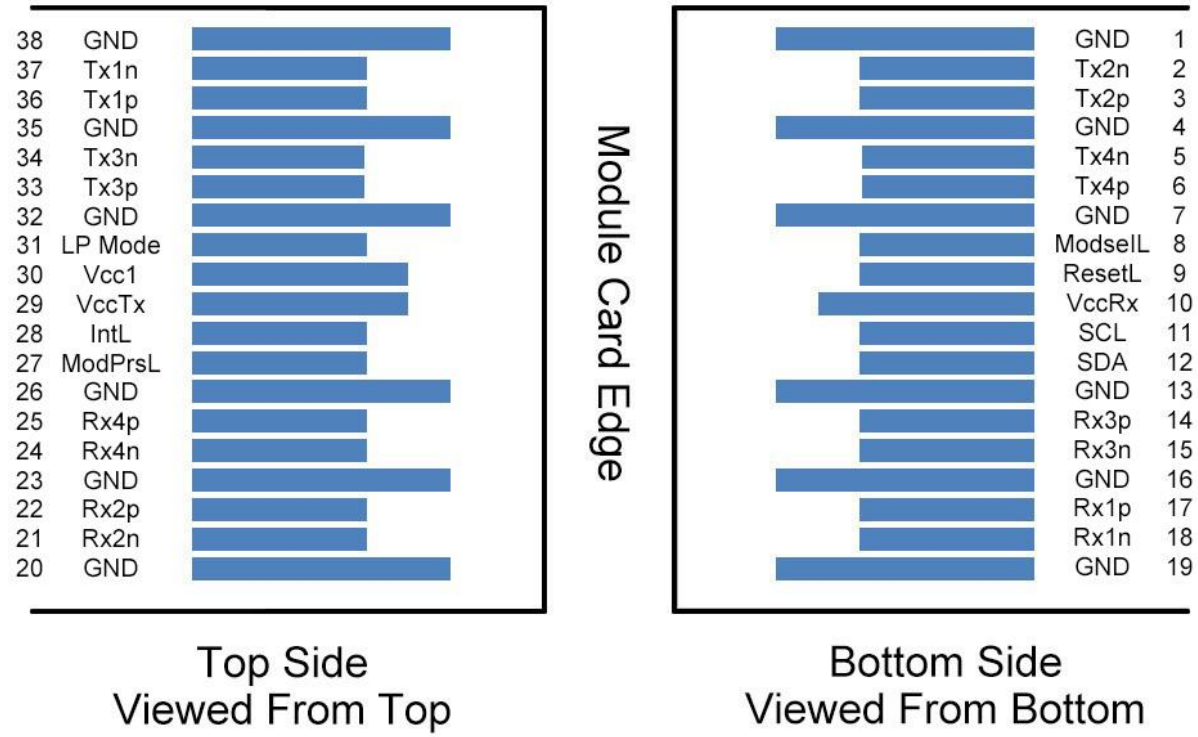
Note4: Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Transceiver Block Diagram



Pin Assignment



Top Side
Viewed From Top

Bottom Side
Viewed From Bottom

Pin Description

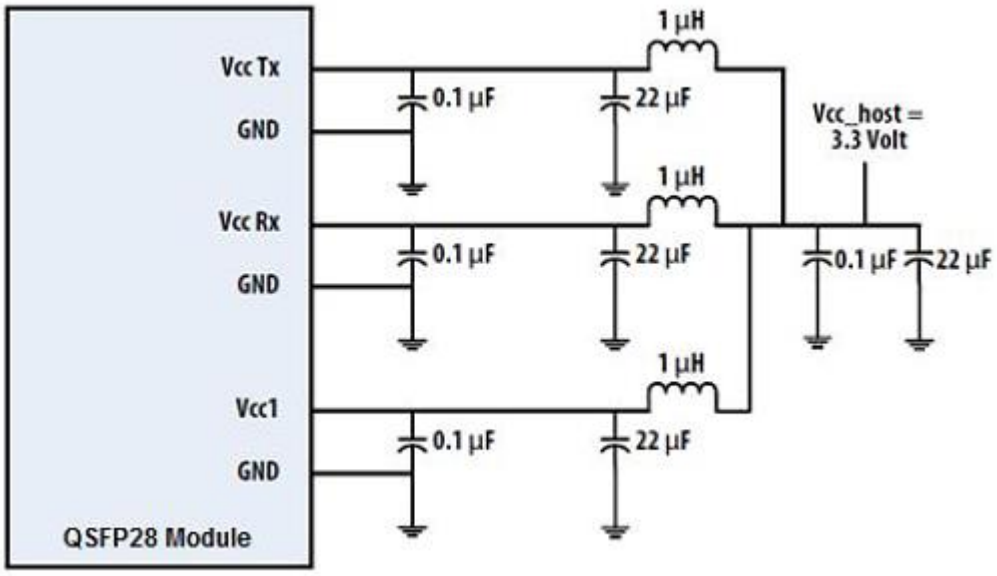
Pin	Logic	Name	Function / Description
1		GND	Module Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Module Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Module Ground
8	LVTLL-I	ModSelL	Module Select
9	LVTLL-I	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data
13		GND	Module Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Module Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Module Ground
20		GND	Module Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Module Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Module Ground
27	LVTLL-O	ModPrsL	Module Present
28	LVTLL-O	IntL	Interrupt
29		VccTx	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTLL-I	LPMode	Low Power Mode
32		GND	Module Ground

33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Module Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Module Ground

Note1: GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground lane.

Note2: VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.

Recommended Power Supply Filter



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Digital Diagnostic Functions

As defined by the QSFP28 MSA, Ficer's QSFP28 transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current (4-Channel)
- Transmitted optical power (4-Channel)
- Received optical power (4-Channel)
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Controller (DDC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP28 transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the QSFP28 transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information including memory map definitions, please see the QSFP28 MSA Specification.

Digital Diagnostic Memory Map

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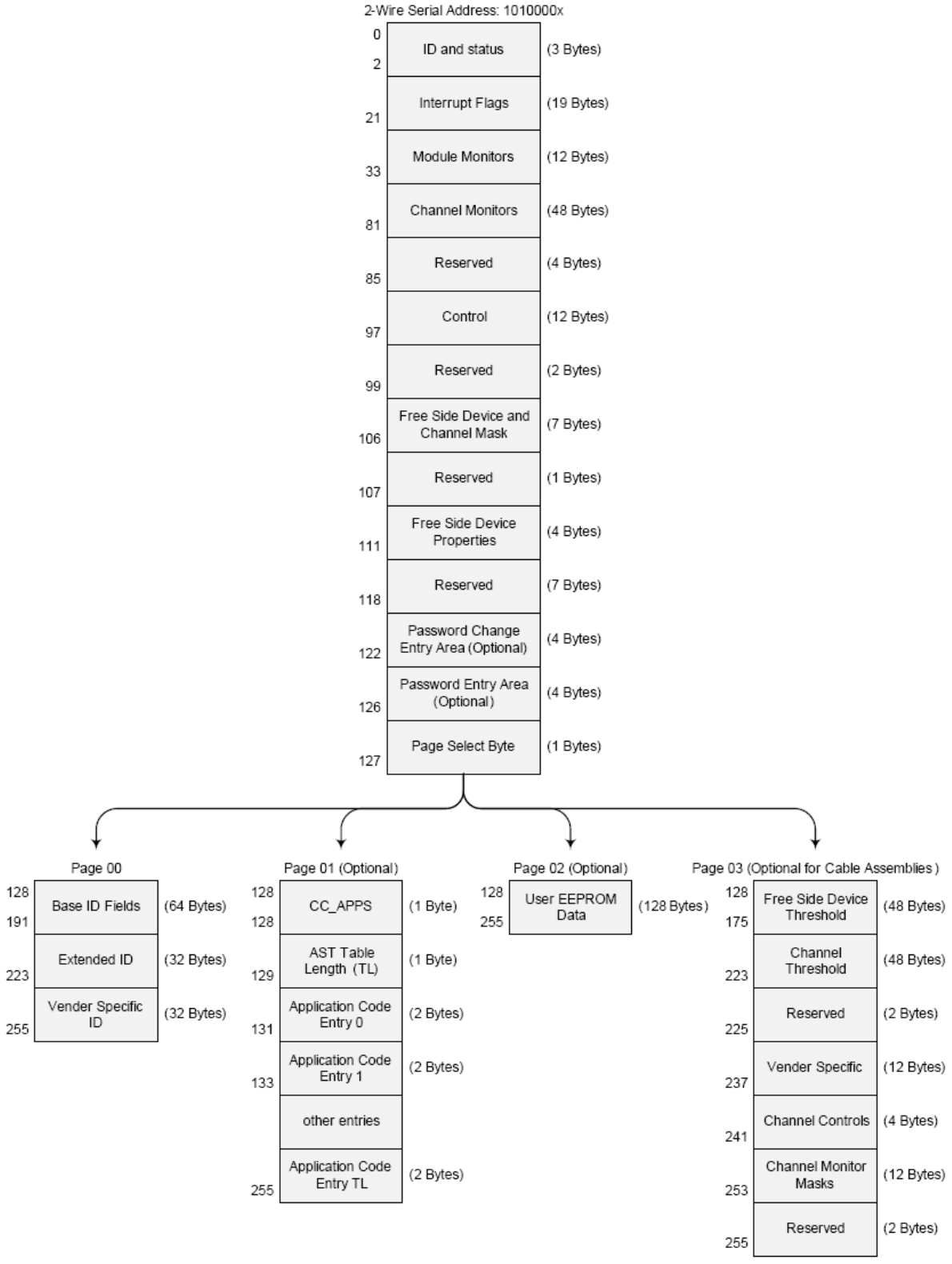
2-Wire Serial Address: 1010000x
0
ID and status
(3 Bytes)
2
Interrupt Flags
(19 Bytes)
21
Module Monitors
(12 Bytes)
33
Channel Monitors
(48 Bytes)
81
Reserved
(4 Bytes)
85
Control
(12 Bytes)
97
Reserved
(2 Bytes)
99
Free Side Device and Channel Mask
(7 Bytes)
106
Reserved
(1 Bytes)
107
Free Side Device Properties
(4 Bytes)
111
Reserved
(7 Bytes)
118
Password Change Entry Area (Optional)
(4 Bytes)
122
Password Entry Area (Optional)
(4 Bytes)
126
Page Select Byte
(1 Bytes)
127
Page 00
128
Base ID Fields
(64 Bytes)
191
Extended ID
(32 Bytes)
223
Vender Specific ID
(32 Bytes)
255
Page 01 (Optional)
128
CC_APPS
(1 Byte)
128
AST Table Length (TL)
(1 Byte)
129
Application Code Entry 0
(2 Bytes)
131
Application Code Entry 1
(2 Bytes)
133
other entries
Application Code Entry TL
(2 Bytes)
255
Page 02 (Optional)
128
User EEPROM Data
(128 Bytes)
255
Page 03 (Optional for Cable Assemblies)
128
Free Side Device Threshold
(48 Bytes)
175
Channel Threshold
(48 Bytes)
223
Reserved
(2 Bytes)
225
Vender Specific
(12 Bytes)
237
Channel Controls
(4 Bytes)
241
Channel Monitor Masks
(12 Bytes)
253
Reserved
(2 Bytes)
255

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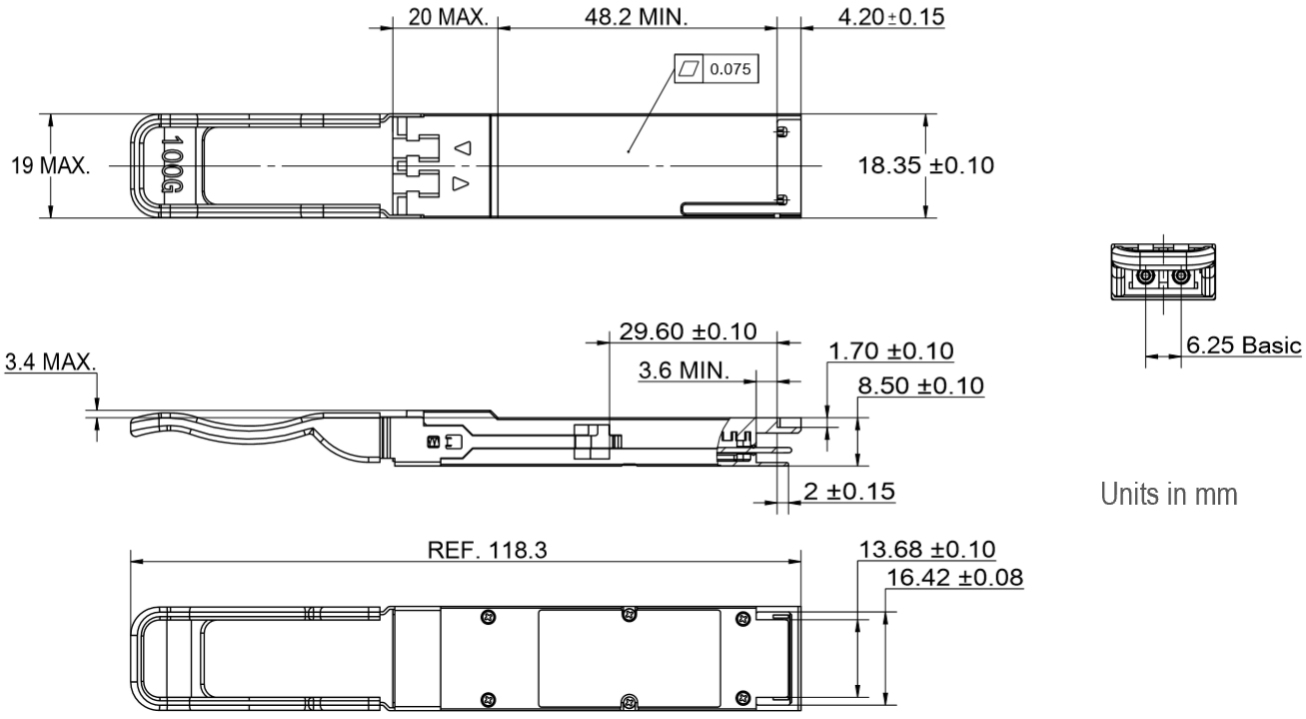
Mechanical Dimensions



(All Dimensions are ±0.20mm Unless Otherwise Specified, Unit: mm)

Ordering Information

Part No.	Tx	Rx	Link	DDM	Temp.
FQ28-K7-L13-80DR	1295.56 nm 1300.05 nm 1304.58 nm 1309.14 nm	1295.56 nm 1300.05 nm 1304.58 nm 1309.14 nm	SMF 80km (with FEC)	Yes	0~70°C

Note: Distances are indicative only. To calculate a more precise link budget based on specific conditions in your application, please refer to the optical characteristics