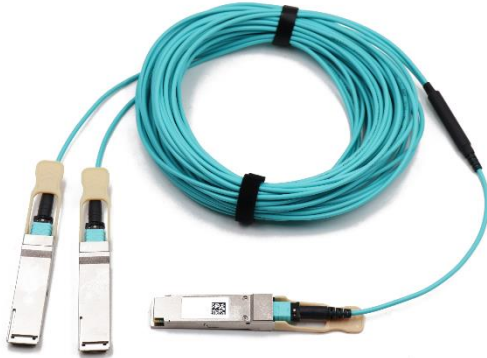




200G QSFP56 to 2x100G QSFP56 Active Optical Cable (AOC) Hot Pluggable, 850nm VCSEL, MMF 1~100M, DDM

Part Number: FAOC-B0G-Q6Q5-xxx-xx



Overview

FAOC-B0G-Q6Q5-xxx-xx 200G QSFP+ Active Optical Cables (AOC) are direct-attach fiber assemblies with QSFP56 form factor. The AOC utilize multi-mode fiber with 850nm VCSEL and PIN PD. It could be used as an alternative solution to 200G QSFP56 to 2x100G QSFP56 passive and active copper cables, while providing improved signal integrity, longer distances, superior electro-magnetic immunity & better bit error rate performance. They are suitable for 1~100 meters distances and offer a cost-effective way for very high port density connections.

Applications

- 200GBASE-SR4 to 2x100GBASE-SR2 Ethernet
- InfiniBand 200Gb/s HDR to 2x100Gb/s HDR100
- Data Center & Storage
- Datacom / Telecom Switch & Router

Features

- Compliant with IEEE 802.3cd 200GBASE-SR4
- Compatible with IEEE 802.3cd 100GBASE-SR2
- Compliant with SFF-8665 for QSFP56 port
- Compliant with IBTA InfiniBand HDR
- 4 independent full-duplex channels
- Aggregate data rate 212.5Gbps
- Hot Pluggable
- 4x50G PAM4 VCSEL / PIN array
- 38-pin electrical edge connector
- CMIS4.0 management interface
- 2-wire interface for management and diagnostic monitor compliant with SFF-8636
- Single 3.3V power supply
- Link distance 100m over OM4 fiber and 70m over MM OM3 fiber
- Low Power Consumption <4.5W
- RoHS Compliant



Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Storage Temperature	T _{ST}	-5	+75	°C
Storage Relative Humidity	RH	5	85	%
Supply Voltage	V _{CC}	-0.5	+3.6	V

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Case Operating Temperature	T _{OP}	0	-	+70	°C	
Supply Voltage	V _{CC}	+3.13	+3.3	+3.47	V	
Bit Rate, per Lane	BR		26.5625		GBd	
Data Rate Accuracy	ΔDR	-100		+100	ppm	
Bit Error Rate (Pre-FEC)	BER			2.4x10 ⁻⁴		1
Power Consumption, per 200G QSFP56	P			4.5	W	2
Power Consumption, per 100G QSFP56	P			2.5	W	2
Power-On Initialization Time				2000	ms	3
Control Input Voltage High	V _{IH}	2		V _{CC} +0.3	V	
Control Input Voltage Low	V _{IL}	-0.3		0.8	V	
Control Output Voltage High	V _{OH}	2		V _{CC} +0.3	V	
Control Output Voltage Low	V _{OL}	-0.3		0.8	V	
Minimum Cable Bending Radius		30			mm	

Note1: Measured with a PRBS 2³¹-1 test pattern @26.5625Gbd PAM4.

Note2: With Retiming on all Lanes.

Note3: Power-on Initialization Time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the module is fully functional.



Transmitter Electro-optical Characteristics

$V_{CC} = 3.13V$ to $3.47V$, $T_{OP} = 0\text{ }^{\circ}C$ to $70\text{ }^{\circ}C$

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Average Launch Power, per Lane	P_{AVG}	-6.0		+4.0	dBm	
Optical Wavelength, each Lane	λ_c	840	850	860	nm	
Spectral Width (RMS)	$\Delta\lambda$			0.6	nm	
Optical Extinction Ratio	ER	3			dB	
Optical Return Loss Tolerance	ORLT			12	dB	
Differential Data Input Voltage	V_{IN-PP}	300		900	mVpp	
Common Mode Noise RMS				17.5	mV	
Common Mode Voltage		-0.4		3.3	V	
Differential termination mismatch				10	%	
DC common mode voltage		-350		2850	mV	

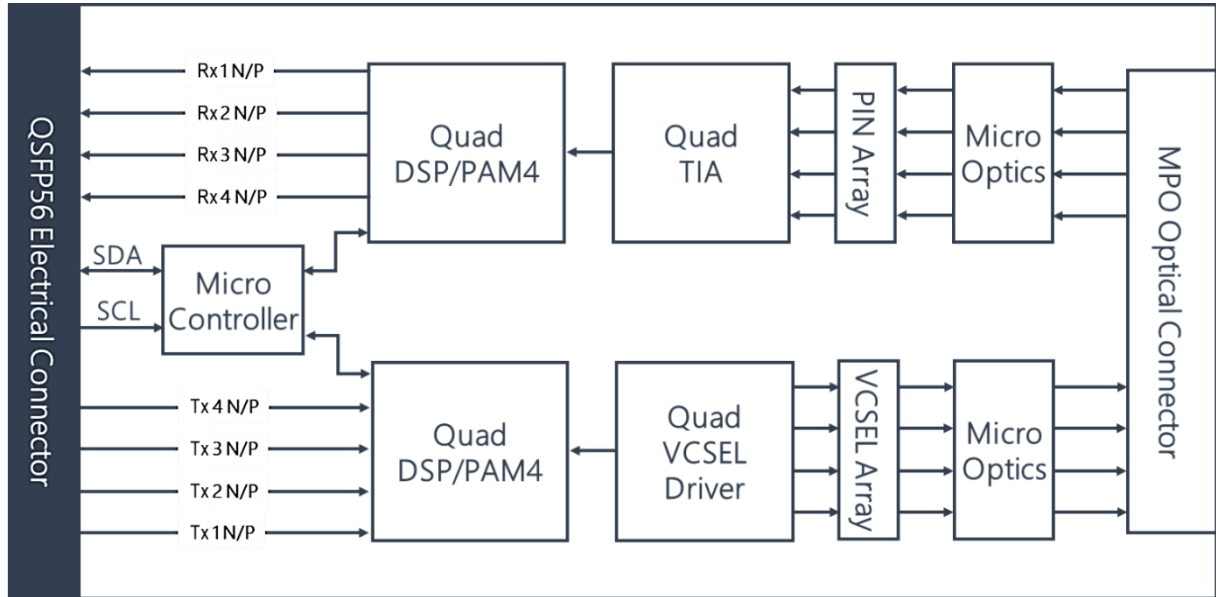
Receiver Electro-optical Characteristics

$V_{CC} = 3.13V$ to $3.47V$, $T_{OP} = 0\text{ }^{\circ}C$ to $70\text{ }^{\circ}C$

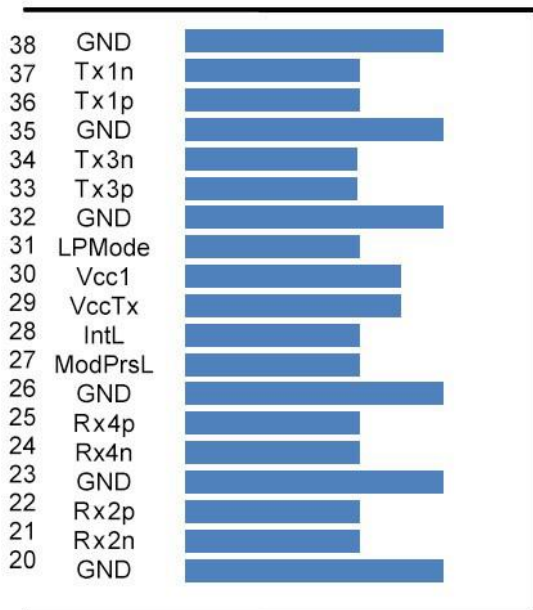
Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Average Receive Power, per Lane	P_{RX-AVG}	-7.9		+4.0	dBm	
Damage Threshold, per Lane	D_{TH}	+5.0			dBm	
Optical Wavelength, each Lane	λ_c	840	850	860	nm	
Receiver Reflectance	R_{RX}			-12	dB	
Differential Data Output Voltage	V_{OUT-PP}	300		900	mVpp	
Differential termination mismatch				10	%	
Transition time (20% to 80%)	T_r, T_f	9.5			ps	
DC common mode voltage		-350		2850	mV	



Transceiver Block Diagram (200G QSFP56)

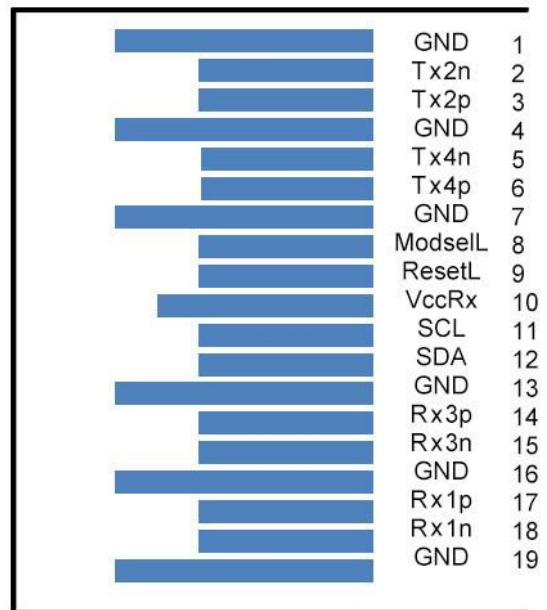


Pin Assignment



Top Side
Viewed From Top

Module Card Edge



Bottom Side
Viewed From Bottom



Pin Description

Pin	Logic	Name	Function / Description
1		GND	Module Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Module Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Module Ground
8	LVTLL-I	ModSelL	Module Select
9	LVTLL-I	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data
13		GND	Module Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Module Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Module Ground
20		GND	Module Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Module Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Module Ground
27	LVTLL-O	ModPrsL	Module Present
28	LVTLL-O	IntL	Interrupt
29		VccTx	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTLL-I	LPMODE	Low Power Mode
32		GND	Module Ground



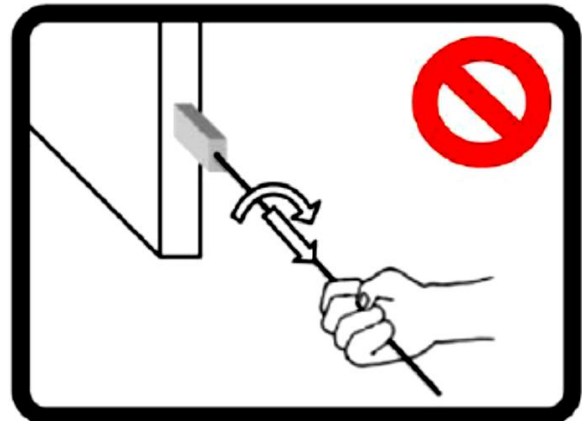
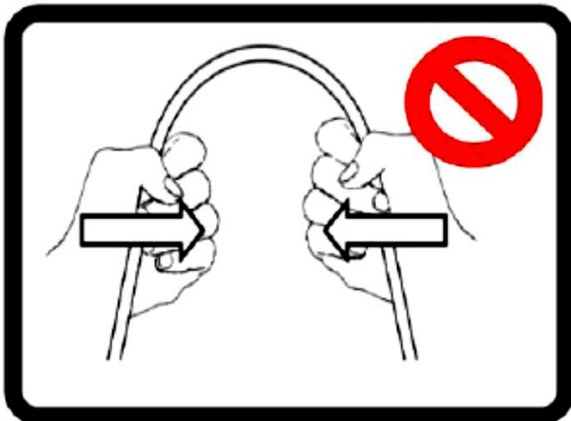
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Module Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Module Ground

Note1: GND is the symbol for signal and supply (power) common for QSFP modules. All are common within the QSFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground lane.

Note2: VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

Handling

Care should be taken to restrict exposure to the conditions defined in the Absolute Maximum Ratings and Recommended Operating Conditions. Put the product in an even and stable location. If the product falls down or drops, it may cause an injury or malfunction. The cable must not be subject to extreme bends during installation or while in operation. If you bend the cable at a radius less than the cable minimum bend radius, then the cable may get damaged. Don't twist or pull by force ends of the cable, which might cause malfunction. In addition, the bending direction should be perpendicular to the flat surface of the ribbon cable. Please do not bend or kink the cable in lateral directions of flat surface of the ribbon.





Digital Diagnostic Functions

As defined by the QSFP MSA (SFF-8636), Ficer's QSFP56 transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

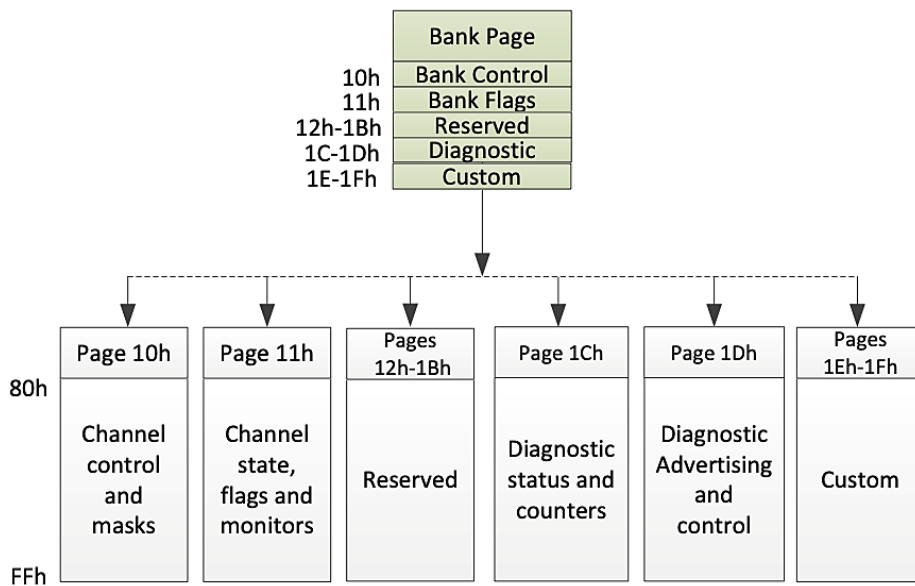
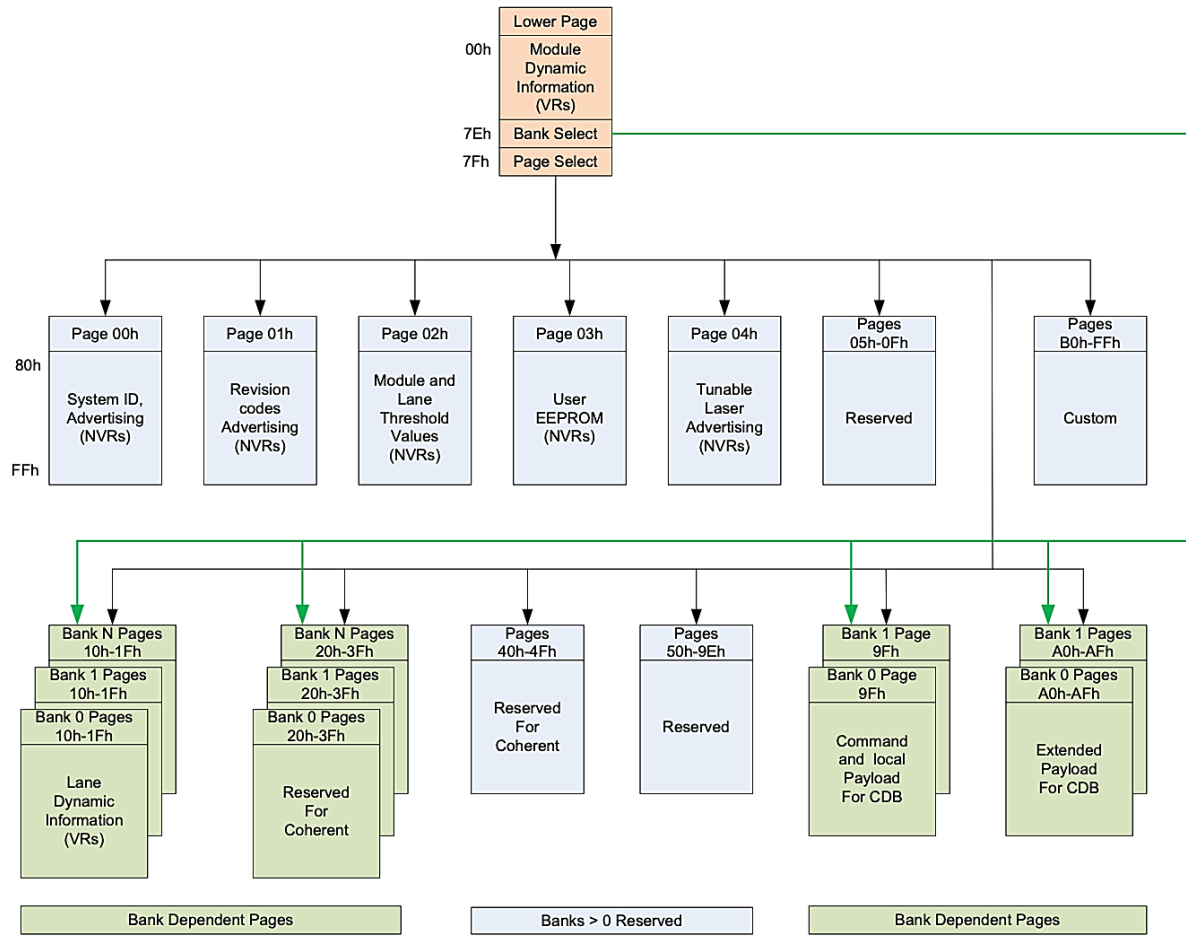
- Transceiver temperature
- Laser bias current (4-Channel)
- Transmitted optical power (4-Channel)
- Received optical power (4-Channel)
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Controller (DDC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP56 transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the QSFP56 transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

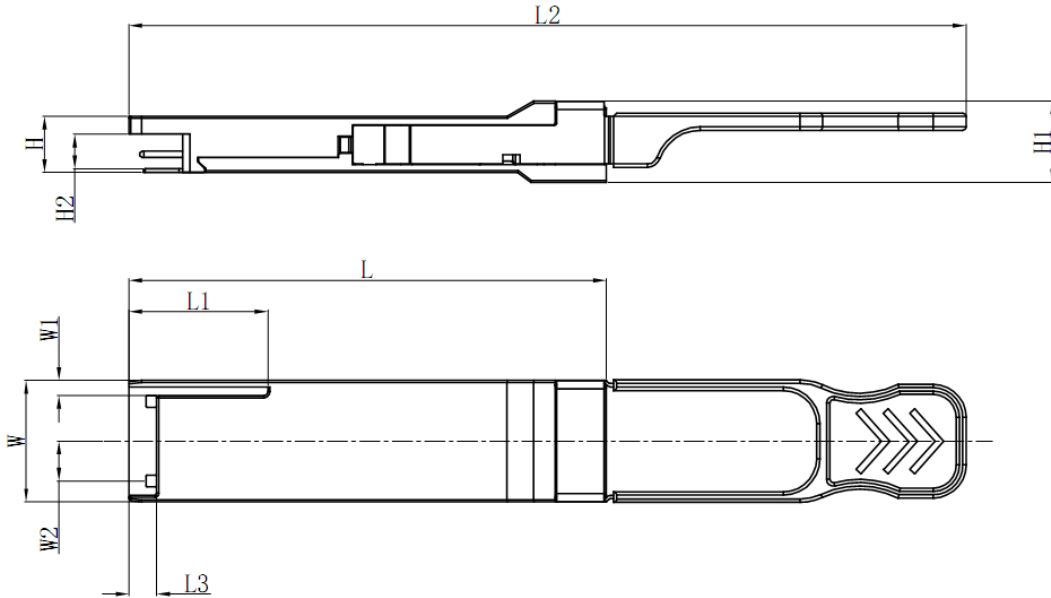
For more detailed information including memory map definitions, please see the QSFP MSA Specification.

Digital Diagnostic Memory Map (compliant QSFP-DD Rev4.0 CMIS)



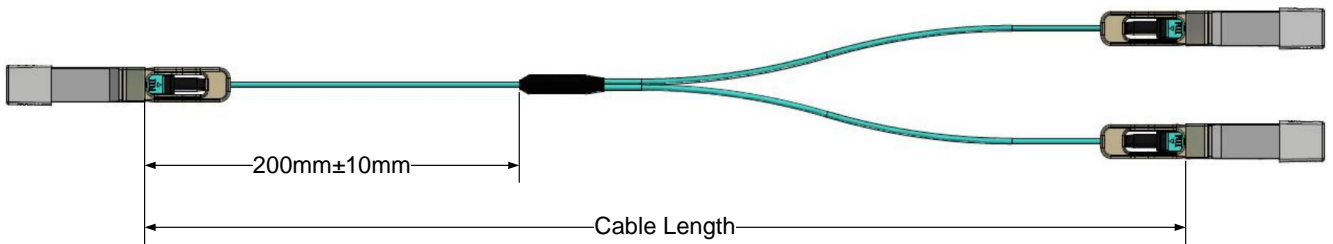


Mechanical Dimensions



	L	L1	L2	L3	L4	W	W1	W2	H	H1	H2
Max	72.2	-	128	4.35	61.4	18.45	-	6.2	8.6	12.4	5.35
Typical	72.0	-	-	4.20	61.2	18.35	-	-	8.5	12.2	5.2
Min	68.8	16.5	124	4.05	61.0	18.25	2.2	5.8	8.4	12.0	5.05

(All Dimensions are $\pm 0.20\text{mm}$ Unless Otherwise Specified, Unit: mm)



Cable Length (CL)	Tolerance
< 1m	+10 / -0cm
1 ~ 4.5m	+15 / -0cm
4.6m ~ 14.5m	+30 / -0cm
14.6m ~ 100m	+2% / -0cm



200Gb/s Side	100Gb/s Side
	Port 1
Tx1	Rx1
Rx1	Tx1
Tx2	Rx2
Rx2	Tx2
	Port 2
Tx3	Rx1
Rx3	Tx1
Tx4	Rx2
Rx4	Tx2

Ordering Information

FAOC-B0G-Q6Q5--L3

Cable Length

meters (including QSFP56)

Example: 003=3m, 015=15m, 100=100m, 0X5=0.5m, 3X5=3.5m

Cable Jacket

P: PVC Q: OFNP

L: LSZH* (default)

Fiber Type

2: MM 50/125 OM2

3: MM 50/125 OM3* (default)

4: MM 50/125 OM4