



## 10G SFP+ Electrical Passive Loopback Hot Pluggable, 0~5dB Internal Attenuation, 0~2.5W Power Consumption

**Part Number:** FSPP-HX-XLB-xx-xx



### Overview

FSPP-HX-XLB SFP+ Loopback modules are compliant with the current SFP+ Multi-Source Agreement (MSA) specification. The Loopback modules provide an effective way of testing the SFP+ port in the host system by looping back the electrical signal (optics are excluded). It provides an economical way to mimic Fast Ethernet, Gigabit Ethernet, 10G Ethernet, SONET OC3~OC192, SDH STM-1~STM-64, 1x/2x/4x/8x/10x Fiber Channel, and CPRI Option #7, #8 on SFP/SFP+ ports in simulation testing environments.

### Applications

- Board and System Level Testing
- System Test and Measurement
- Switch / Router Chamber Test
- Power Consumption Validation

### Features

- Compliant with SFF-8431 SFP+ MSA
- Electrical Data Rate up to 10.5Gbps
- Hot Pluggable
- 2-wire interface for management
- Single +3.3V power supply
- Different Option for Internal Attenuation and Power Consumption
- RoHS Compliant

### Absolute Maximum Ratings

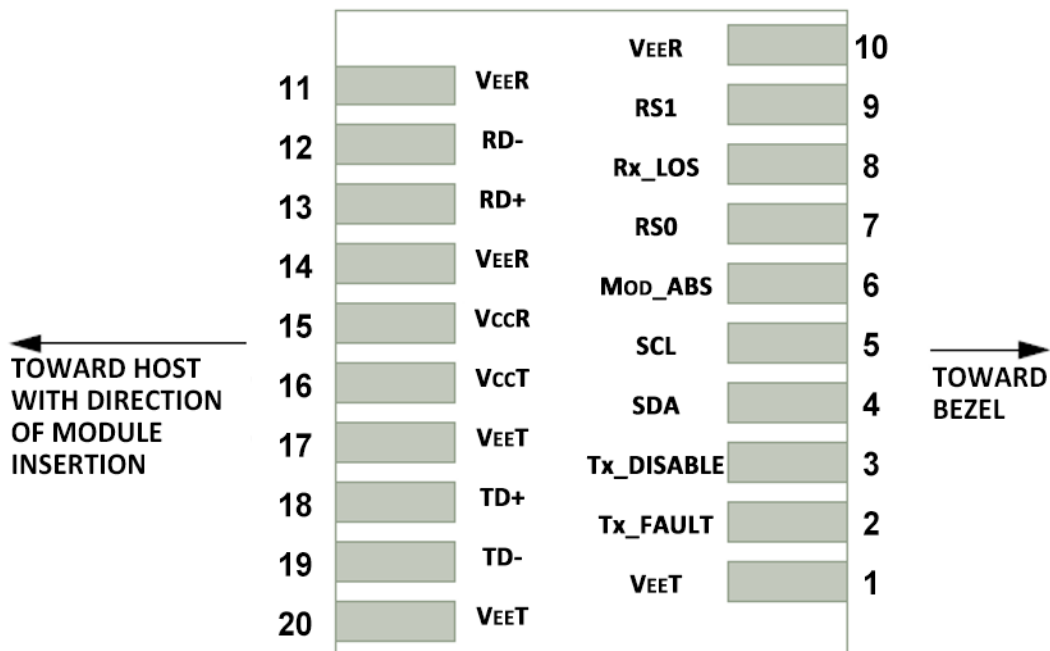
Parameters	Symbol	Min.	Max.	Unit
Storage Temperature	T <sub>ST</sub>	-40	+85	°C
Storage Relative Humidity	RH	0	95	%
Supply Voltage	V <sub>CC3</sub>	-0.5	+4.0	V



## Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Unit
Case Operating Temperature	T <sub>OP</sub>	-20	-	+85	°C
Supply Voltage	V <sub>CC</sub>	+3.13	+3.3	+3.47	V
Date Rate	DR	0.1	-	10.5	Gb/s
Differential Impedance	Z	90	100	110	Ohm
Durability Cycles			100	200	Times

## Pin Assignment



Host PCB SFP28 Pad Assignment Top View

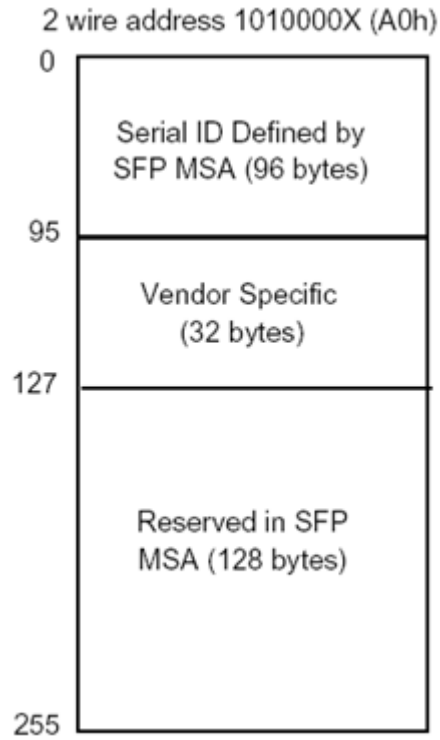


## Pin Description

Pin	Name	Function / Description
1	VEET	Transmitter Ground
2	Tx_FAULT	Internally tied to Transmit ground. Tx_FAULT is not implemented.
3	Tx_DISABLE	Internally pulled up to Vcc through a 5.11k ohm resistor. Tx_DISABLE is not implemented.
4	SDA	2-wire Serial Interface Data Line (SDA: Serial Data Signal)
5	SCL	2-wire Serial Interface Clock (SCL: Serial Clock Signal)
6	MOD_ABS	Module Absent, this pin is internally tied to Transmit ground
7	RS	Rate Select, this Pin is internally pulled low through a 33.2k resistor. Rate Select is not implemented.
8	Rx_LOS	Receiver Loss of Signal Indication, this Pin Internally tied to Receiver Ground. Rx_LOS is not implemented.
9	VEER	Receiver Ground
10	VEER	Receiver Ground
11	VEER	Receiver Ground
12	RD-	Receiver Inverted Data output, AC coupled
13	RD+	Receiver Non-Inverted Data output, AC coupled
14	VEER	Receiver Ground
15	VCCR	Not used
16	VcCT	EEPROM power
17	VEET	Transmitter Ground
18	TD+	Transmitter Non-Inverted Data Input, AC coupled
19	TD-	Transmitter Inverted Data Input, AC coupled
20	VEET	Transmitter Ground

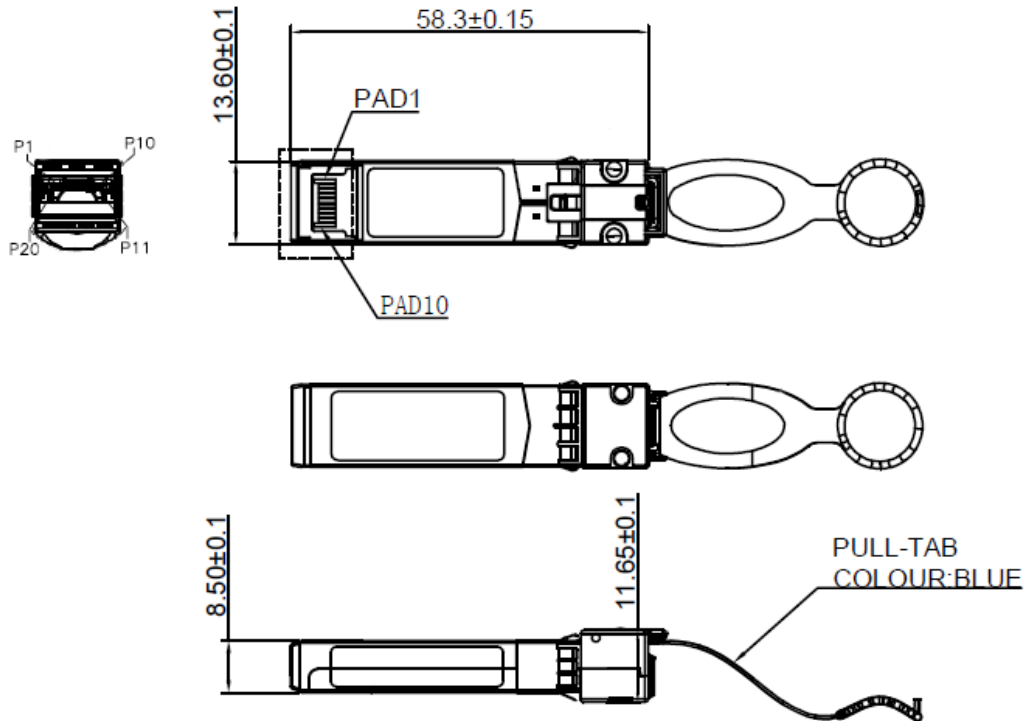


## Memory Map





## Mechanical Dimensions



(All Dimensions are ±0.20mm Unless Otherwise Specified, Unit: mm)

## Ordering Information

FSP-PHX-XLB-□□-□□

### Internal Attenuation

00: 0dB                      35: 3.5dB  
 50: 5dB                     xx: Customized Value

### Power Consumption

00: 0W                      10: 1W  
 15: 1.5W                  20: 2W  
 25: 2.5W                  xx: Customized Value